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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,955	11/20/2003	Ha C. Vu	08211/0200374-US0	9020

38845 7590 12/01/2004

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,955	VU, HA C.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6, 7, and 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Razavi (RF MICROELECTRONICS, Prentice Hall Communications Engineering and Emerging Technologies Series, Chapter 8, pp 270-271, 1997).

With regard to claims 1 and 10, Razavi discloses in Figs. 8.27 & 8.28 a circuit for dividing periodic input pulses by a preset integer M, and a method of use thereof, comprising a dual modulus prescaler (Prescaler) arranged to receive periodic input pulses (fin) and to count the received input pulses for generating prescaled pulses, wherein one prescaled pulse is generated for every Qth input pulse, wherein Q is a division modulus having a value depending on a value of a modulus control signal, wherein when a prescaled pulse is generated from a selected input pulse, the modulus control signal is ignored at least until the onset of a next input pulse is received (see page 270, 3rd paragraph); and a swallow counter (Swallow Counter) arranged to change the modulus control signal (Modulus Control) to a different value in response to the prescaler receiving every Mth input pulse (see page 270, 2nd paragraph), wherein M is a preset integer; and a program counter to generate a reset signal in response to the prescaler receiving the Mth input pulse, and wherein the swallow counter changes the modulus control signal in response to the reset signal (see page 270, 3rd paragraph).

With regard to claims 2, 3, 11-14, the reference also meets the recited limitations in these claims (see page 270, 1st & 2nd paragraphs).

With regard to claims 6 and 15, a frequency/phase detector (PD) arranged to receive a divided down signal generated in response to the prescaler receiving the Mth input pulse, and to output a synchronized signal in response to the divided down signal (see page 270, 1st & 2nd paragraphs); and a fast clock generator (VCO) to generate a fast clock signal (fout) from the synchronized signal, and wherein the input pulses are derived from the fast clock signal.

With regard to claim 7, the program counter (Program Counter) is adapted to generate the reset signal (Reset) in response to receiving a prescaled pulse that corresponds to the prescaler receiving the Mth input pulse (also see page 270, 2nd & 3rd paragraphs).

Claim 9 is similarly rejected; note the above discussion with regard to claims 1 and 10.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 8 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Razavi in view of Sudjian (US Pat. 6,737,899).

With regard to claim 4, the above discussed circuit of Razavi meets all of the claimed limitations except for the limitation that Razavi does not disclose the prescaler in details. Sudjian teaches in Fig. 10 a prescaler circuit (1030) including an OR gate (1034c) for ORing the

modulus control signal (MODE) with another signal. Therefore, it would have been obvious to one of ordinary skill in the art to implement the prescaler circuit taught by Sudjian with the prior art (Figs. 8.27 & 8.28 of Razavi) in order to meet the specific condition of the particular application.

With regard to claim 8, the above discussed circuit of Razavi meets all of the claimed limitations except for the limitation that Razavi does not disclose the prescaler being initialized. Sudjian teaches in Figs. 9A-9B a prescaler circuit (910) being initialized by to particular values when a prescaled pulse is generated (column 11, lines 1-35). Therefore, it would have been obvious to one of ordinary skill in the art to implement that initialization process taught by Sudjian with the prior art (Figs. 8.27 & 8.28 of Razavi) in order to reset the prescaler at a predetermined values, including when a Power On Reset is performed.

With regard to claim 17, the above discussed circuit of Razavi meets all of the claimed limitations except for the limitation that Razavi does not disclose the prescaler in details such as the state variables are encoded in signals generated by logical devices. Sudjian teaches in Fig. 9A a prescaler circuit having the state variables are encoded in signals generated by logical devices (912-918). Therefore, it would have been obvious to one of ordinary skill in the art to implement the prescaler taught by Sudjian with the prior art (Figs. 8.27 & 8.28 of Razavi) in order to generate the state variables in order to meet the specific condition of the particular application.

Claims 18 and 19 are similarly rejected; note the above discussion with regard to claims 4 and 8.

With regard to claim 20, the above discussed circuit of Razavi meets all of the claimed limitations except for the limitation that Razavi does not disclose the prescaler in details how the vector (output signal of Prescaler) is made such as from state variables D2, D1, D0. Sudjian teaches in Figs. 9A & 10 a prescaler circuit having the vector that is made in different ways. Therefore, it would have been obvious to one of ordinary skill in the art to implement that teaching of Sudjian with the prior art (Figs. 8.27 & 8.28 of Razavi) in order to generate the vector of the prescaler with a certain combination in order to meet the specific condition of the particular application.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
November 19, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800